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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,930	07/07/2003	Shigeyuki Aino	Q76415	6921

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EXAMINER	
TRUONG, LOAN	
ART UNIT	**PAPER NUMBER**
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,930	AINO ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,9-15 and 20-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-15 and 20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Request for Continuation filled on February 13, 2007 in application 10/612,930.

2. Examiner acknowledged that claims 1-4, 9-15 and 20-22 are presented for examination; Claims 1 and 12 are amended to overcome the 35 U.S.C. 112 rejection. Claims 5-8, 16-19 and 23-24 are cancelled.

Response to Arguments

3. Applicant's arguments with respect to claims 1-4, 9-15 and 20-22 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 and 12 reference "said processor" being in singular form cannot sent address strobes to monitor element in the same cycle for determining synchronism. Examiner suggest said processor be clarified to plurality form referring to first and second processor.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-4, 9-15 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (EP 0817053 A1) in further view of McDonald (US 5,249,188).

In regard to claim 1, Williams et al. disclosed an information processing apparatus comprising:

first and second computer elements (*identical processing sets, fig. 1, 10, 11, 12)* which execute the same instructions substantially simultaneously in substantial synchronism (*operate in synchronism under a common clock, col. 1 lines 10-16)*, and which have first and second memory elements (*internal state storage memory, fig. 2, 22, col. 1 lines 16-20)*, respectively, wherein said first and second memory (*internal state storage memory, fig. 2, 22, col. 1 lines 16-20)* store first and second data (*first recording mechanism can be activated to record memory*

update events and a second recording mechanism record at least a limited number of memory updates, fig. 3, 25, 26, col. 2 lines 39-43), respectively;

a monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* which finds which of said computer elements is out of said synchronism (*output differ, col. 1 lines 34-48)*;

a third memory element (*dirty RAM storage, fig. 4, 46, col. 8 lines 5-18, write buffer for secondary dirty page record, col. 10 lines 29-32)* which stores an address (*first-in-first-out buffer stores up to a predetermined number of update addresses, col. 4 lines 12-19)* directed by a write access request (*copying the contents of the main memory from a running system to the out-of-sync processing set, col. 2 lines 27-30)* at the time when said monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds that said first computer element is out of said synchronism (*output from the processing sets differ, col. 1 lines 34-37)* and thereafter ; and

a copy element (*reintegration mechanism, fig. 3, 27, col. 6 lines 1-7)* which copies third data (*reintegrating the other out-of-sync using software log, col. 5 lines 1-2)* associated with said address or addresses out of said second data stored in said second memory (*first-in-first-out buffer stores up to a predetermined number of update addresses, col. 4 lines 12-19)* to said first memory element when said monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds that said first computer is out of said synchronism (*output from the processing sets differ, col. 1 lines 34-37).*

Wherein said monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* is connected to a bus (*internal bus, fig. 1, 13, col. 1 lines 20-25)* which is directly connected to a processor of said first and second computer elements (*identical processing sets, fig. 1, 10, 11, 12)*;

Williams et al. does not teach the apparatus comprising of a monitor element receiving address strobes from said processor during the same cycle in order to determine whether said first computer element is out of said synchronism.

McDonald teach the apparatus of synchronizing two processor as an integral part of fault detection by implementing a master and a slave processors to resynchronized at every bus cycle by conditioning the processors' READY signal with the ADS (address status) signals from each processor wherein ADS indicates that an access cycle has begun and a valid address is present on the address bus. Furthermore, if a predetermined amount of time passes before both ADS signals are received then the processors are signaled to continue with the cycle and because the processors are no longer synchronized, the buses will miscompare, thereby detecting a fault *(abstract)*.

It would have been obvious to modify the apparatus of William et al. and Prabhu by adding Phelps memory subsystem including an error detection mechanism for address and control signal. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would provide a means of synchronizing two or more processors and thereby allowing detection of faults in a processor CPU system *(col. 1 lines 47-50)*.

In regard to claim 2, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said copy element *(reintegration mechanism, fig. 3, 27, col. 6 lines 1-7)* is activated *(less traumatic out-of-sync events, col. 2 lines 20-23)* unless a permanent failure *(failure of a single processing set, col. 2 lines 10-19)* occurred in said first computer element

(out-of-sync processor, col. 6 lines 1-6).

In regard to claim 3, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said monitor element *(fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds that said first computer element *(out-of-sync processor, col. 6 lines 1-6)* is out of said synchronism *(output differ, col. 1 lines 34-48)* based on the time in which it receives first signals from all of said computer modules *(identical processing sets, fig. 1, 10, 11, 12).*

In regard to claim 4, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said monitor element *(fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds that said first computer element *(out-of-sync processor, col. 6 lines 1-6)* is out of said synchronism *(output differ, col. 1 lines 34-48)* based on the time *(identical output, col. 1 lines 26-37)*, commands *(commands from the processing sets, fig. 1, 10, 11, 12, col. 1 lines 26-37)* and addresses of requests *(address decoder, fig. 9, 91, col. 11 lines 16-28)* from all of said computer modules *(identical processing sets, fig. 1, 10, 11, 12).*

In regard to claim 9, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said third memory element stores *(dirty RAM storage, fig. 4, 46, col. 8 lines 5-18)* an address or addresses *(first-in-first-out buffer stores up to a predetermined number of update addresses, col. 4 lines 12-19)* which is directed when contents of a cache *(write buffer for secondary dirty page record, col. 10 lines 29-32)* is written to said memory

element (*internal state storage memory, fig. 2, 22, col. 1 lines 16-20).*

In regard to claim 10, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said address (*first-in-first-out buffer stores up to a predetermined number of update addresses, col. 4 lines 12-19)* indicates the location (*dirty RAM storage, fig. 4, 46, col. 8 lines 5-18)* in said first memory (*out-of-sync processor, col. 6 lines 1-6)* which has possibility of inconsistency (*pages have been modified by the out-of-sync processor, col. 8 lines 5-18)* with said second memory (*internal state storage memory, fig. 2, 22, col. 1 lines 16-20).*

In regard to claim 11, Williams et al. disclosed the information processing apparatus as claimed in claim 1, wherein said copy element (*reintegration mechanism, fig. 3, 27, col. 6 lines 1-7)* copies said part of the data (*copy corresponding memory portion, col. 6 lines 1-6)* by utilizing a direct memory transmission (*copying contents of main memory from running system to out-of-sync processing sets, col. 2 lines 27-48).*

In regard to claim 12, Williams et al. disclosed an information processing apparatus comprising:

first and second computer elements (*identical processing sets, fig. 1, 10, 11, 12)* which execute the same instructions substantially simultaneously in substantial synchronism (*operate in synchronism under a common clock, col. 1 lines 10-16)*, which have first and second memory elements (*internal state storage memory, fig. 2, 22, col. 1 lines 16-20)*, respectively, and each of which has at least one processor (*processor, fig. 3, 20)* and a bus (*internal bus, fig. 3, 23)*

connected to said processor, wherein said first and second memory (*internal state storage memory, fig. 2, 22, col. 1 lines 16-20)* store first and second data, respectively (*first recording mechanism can be activated to record memory update events and a second recording mechanism record at least a limited number of memory updates, fig. 3, 25, 26, col. 2 lines 39-43)*;

a monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* which is connected to said bus (*internal bus, fig. 3, 23)* and which finds which of said computer elements is out of said synchronism (*output differ, col. 1 lines 34-48)*;

a third memory element (*dirty RAM storage, fig. 4, 46, col. 8 lines 5-18, write buffer for secondary dirty page record, col. 10 lines 29-32)* which an address accessing by a write access request (*copying the contents of the main memory from a running system to the out-of-sync processing set, col. 2 lines 27-30)* at the time when said monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds that said first computer element is out of said synchronism (*output from the processing sets differ, col. 1 lines 34-37)* and thereafter; and

a copy element (*reintegration mechanism, fig. 3, 27, col. 6 lines 1-7)* which copies third data (*reintegrating the other out-of-sync using software log, col. 5 lines 1-2)* associated with said address or addreses out of said second data stored in said second memory (*first-in-first-out buffer stores up to a predetermined number of update addresses, col. 4 lines 12-19)* to said first memory element when said monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds that said first computer element is out of said synchronism (*output from the processing sets differ, col. 1 lines 34-37).*

Williams et al. does not teach the apparatus comprising of a monitor element receiving address strobes from said processor during the same cycle in order to determine whether said first computer element is out of said synchronism.

McDonald teach the apparatus of synchronizing two processor as an integral part of fault detection by implementing a master and a slave processors to resynchronized at every bus cycle by conditioning the processors' READY signal with the ADS (address status) signals from each processor wherein ADS indicates that an access cycle has begun and a valid address is present on the address bus. Furthermore, if a predetermined amount of time passes before both ADS signals are received then the processors are signaled to continue with the cycle and because the processors are no longer synchronized, the buses will miscompare, thereby detecting a fault (*abstract).*

Refer to claim 1 for motivational statement.

In regard to claim 13, Williams et al. disclosed the information processing apparatus as claimed in claim 12, wherein said copy element (*reintegration mechanism, fig. 3, 27, col. 6 lines 1-7)* is activated (*less traumatic out-of-sync events, col. 2 lines 20-23)* unless a permanent failure (*failure of a single processing set, col. 2 lines 10-19)* occurred in said first computer element (*out-of-sync processor, col. 6 lines 1-6).*

In regard to claim 14, Williams et al. disclosed the information processing apparatus as claimed in claim 12, wherein said monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds that said first computer element (*out-of-sync processor, col. 6 lines 1-6)* is out

of said synchronism (*output differ, col. 1 lines 34-48)* based on the time in which it receives first signals from all of said computer modules (*identical processing sets, fig. 1, 10, 11, 12).*

In regard to claim 15, Williams et al. disclosed the information processing apparatus as claimed in claim 12, wherein said monitor element (*fault detector unit voter, fig. 1, 17, col. 1 lines 27-37)* finds that said first computer element (*out-of-sync processor, col. 6 lines 1-6)* is out of said synchronism (*output differ, col. 1 lines 34-48)* based on the time (*identical output, col. 1 lines 26-37)*, commands (*commands from the processing sets, fig. 1, 10, 11, 12, col. 1 lines 26-37)* and addresses of requests (*address decoder, fig. 9, 91, col. 11 lines 16-28)* from all of said computer modules (*identical processing sets, fig. 1, 10, 11, 12).*

In regard to claim 20, Williams et al. disclosed the information processing apparatus as claimed in claim 12, wherein said third memory element stores (*dirty RAM storage, fig. 4, 46, col. 8 lines 5-18)* an address or addresses (*first-in-first-out buffer stores up to a predetermined number of update addresses, col. 4 lines 12-19)* which is directed when contents of a cache *(write buffer for secondary dirty page record, col. 10 lines 29-32)* is written to said memory element (*internal state storage memory, fig. 2, 22, col. 1 lines 16-20).*

In regard to claim 21, Williams et al. disclosed the information processing apparatus as claimed in claim 12, wherein said address or addresses (*first-in-first-out buffer stores up to a predetermined number of update addresses, col. 4 lines 12-19)* indicates the location (*dirty RAM storage, fig. 4, 46, col. 8 lines 5-18)* in said first memory (*out-of-sync processor, col. 6 lines 1-6)*

which has possibility of inconsistency (*pages have been modified by the out-of-sync processor, col. 8 lines 5-18)* with said second memory (*internal state storage memory, fig. 2, 22, col. 1 lines 16-20).*

In regard to claim 22, Williams et al. disclosed the information processing apparatus as claimed in claim 12, wherein said copy element (*reintegration mechanism, fig. 3, 27, col. 6 lines 1-7)* copies third data (*copy corresponding memory portion, col. 6 lines 1-6)* by utilizing a direct memory transmission (*copying contents of main memory from running system to out-of-sync processing sets, col. 2 lines 27-48).*

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Loan Truong whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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